CA-IS36xx High-performance, 5000-V_{RMS} Reinforced Digital Isolators with Integrated high-efficiency, Low-emissions DC-DC Converter

1 Key Features

- Signal rate: DC to 150 Mbps
- Default output: high and low options
- Precise timing (typical @ 5 V supply)
  - 8 ns propagation delay
  - 1 ns pulse Width distortion
  - 2 ns propagation delay skew
  - 5 ns minimum pulse width
- High CMTI: ±150 kV (typical)
- Tri-state outputs with enable
- Schmitt trigger inputs
- Wide input supply range: 3 V to 5.5 V
- Wide operating temperature range: -55° C to 125 °C
- Integrated high-efficiency DC-DC converter with on-chip transformer
  - Regulated output options: 3.3 V or 5.0 V
  - Soft-start to limit inrush current and overshoot
  - Overload and short-circuit protection
  - Thermal shutdown
- Robust electromagnetic compatibility (EMC)
  - Low emissions
- Robust isolation barrier:
  - Isolation rating up to 5.0 kV_{RMS}
  - Isolation Barrier Life: > 40 Years
- RoHS-Compliant Packages
  - SOIC16 Wide Body

2 Applications

- Industrial automation systems
- Motor control
- Medical equipment
- Test and measurement
- Isolated ADC, DAC

3 Description

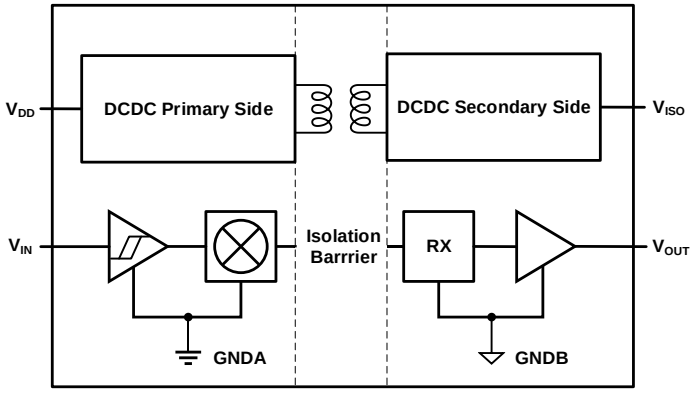
The CA-IS36xx is a family of high-performance reinforced digital isolators with an integrated isolated DC-DC converter. The CA-IS36xx eliminate the need for a separate, isolated power supply, which results in a small form factor, total isolation solution.

The CA-IS3620/ CA-IS3621/ CA-IS3622 are dual-channel digital isolators. And the CA-IS3640/ CA-IS3641/ CA-IS3642/ CA-IS3643/ CA-IS3644 are quad-channel digital isolators. The CA-IS3620 device has two channels in the same direction, the CA-IS3621 and CA-IS3622 device has one forward and one reverse-direction channels, as shown in Figure 7-1. The CA-IS3640 device has all four channels in the forward direction, the CA-IS3641 device has three forward and one reverse-direction channels, the CA-IS3642 device has two forward and two reverse-direction channels, the CA-IS3643 device has one forward and three reverse-direction channels, and the CA-IS3640 device has all four channels in the reversed direction, as shown in Figure 7-2. All devices have fail-safe mode option. If the input signal is lost, default output is low for devices with suffix L and high for devices with suffix H.

Device Information

PART NUMBER	PACKAGE	BODY SIZE(NOM)
CA-IS3620, CA-IS3621, CA-IS3622, CA-IS3640, CA-IS3641, CA-IS3642, CA-IS3643, CA-IS3644	SOIC16-WB(W)	10.30 mm × 7.50 mm

Simplified Functional Diagram

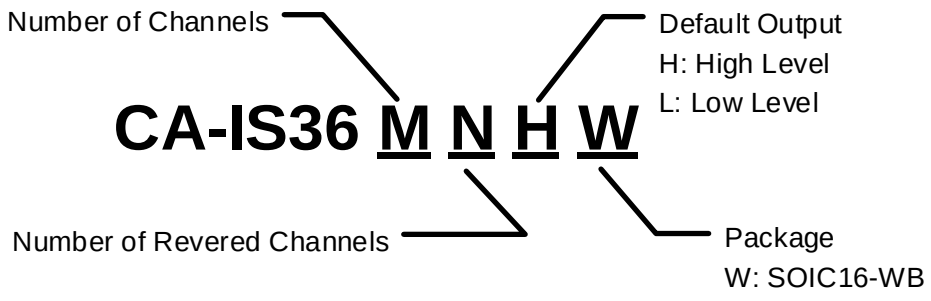


4 Ordering Guide

Table 4-1 Ordering Guide for Valid Ordering Part Number

Ordering Part Number	Number of Inputs A Side	Number of Inputs B Side	Default Output	Isolation Rating (kV)	Package
CA-IS3620L	2	0	Low	5.0	SOIC16-WB
CA-IS3620H	2	0	High	5.0	SOIC16-WB
CA-IS3621L	1	1	Low	5.0	SOIC16-WB
CA-IS3621H	1	1	High	5.0	SOIC16-WB
CA-IS3622L	0	2	Low	5.0	SOIC16-WB
CA-IS3622H	0	2	High	5.0	SOIC16-WB
CA-IS3640L	4	0	Low	5.0	SOIC16-WB
CA-IS3640H	4	0	High	5.0	SOIC16-WB
CA-IS3641L	3	1	Low	5.0	SOIC16-WB
CA-IS3641H	3	1	High	5.0	SOIC16-WB
CA-IS3642L	2	2	Low	5.0	SOIC16-WB
CA-IS3642H	2	2	High	5.0	SOIC16-WB
CA-IS3643L	1	3	Low	5.0	SOIC16-WB
CA-IS3643H	1	3	High	5.0	SOIC16-WB
CA-IS3644L	0	4	Low	5.0	SOIC16-WB
CA-IS3644H	0	4	High	5.0	SOIC16-WB

5 Name Convention



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6 Revision History

Revision 0: Preview version.

7 PIN Descriptions and Functions

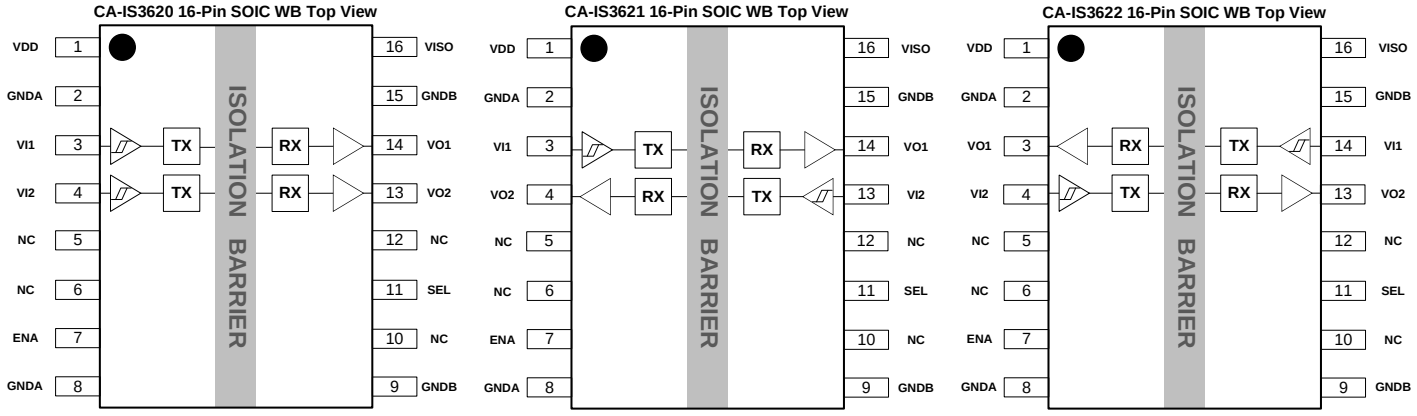


Figure 7-1 CA-IS362x Top View

Table 7-1 CA-IS364x Pin Description and Functions

Name	SOIC16 Pin#	Type	Description
VDD	1	Supply Input	Side A power supply
GNDA	2	Ground	Side A ground
VI1 / VO1	3	Digital I/O	Side A digital input for CA-IS3620 / CA-IS3621 or output for CA-IS3622
VI2 / VO2	4	Digital I/O	Side A digital input for CA-IS3620 / CA-IS3622 or output for CA-IS3621
NC[1]	5	No Connection	Not Connected
NC	6	No Connection	Not Connected
ENA[2]	7	Digital Input	Output enable for side A
GNDA	8	Ground	Side A ground
GNDB	9	Ground	Side B ground
NC	10	No Connection	Not Connected
SEL[3]	11	Digital Input	VISO selection pin
NC	12	No Connection	Not Connected
VI2 / VO2	13	Digital I/O	Side B digital input for CA-IS3621 or output for CA-IS3620 / CA-IS3622
VI1 / VO1	14	Digital I/O	Side B digital input for CA-IS3622 or output for CA-IS3620 / CA-IS3621
GNDB	15	Ground	Side B ground
VISO	16	Supply Output	Isolated output supply voltage determined by SEL pin

1. No Connect. These pins are not internally connected. They can be left floating, tied to VDD or tied to GND.
2. Enable input ENA can be used for multiplexing, for clock sync, or other output control. ENA logic operation is summarized for each isolator product in Table 10-3. This input is internally pulled-up to local VDD allowing them to be connected to an external logic level (high or low) or left floating. To minimize noise coupling, do not connect circuit traces to ENA if it is left floating. If ENA is unused, it is recommended to be connected to an external logic level, especially for the CA-IS362x operating in a noisy environment.
3. VISO selection pin. VISO = 5 V when SEL is connected to VISO. VISO = 3.3 V, when SEL is connected to GNDA or left floating. SEL operation is summarized in Table 10-1.

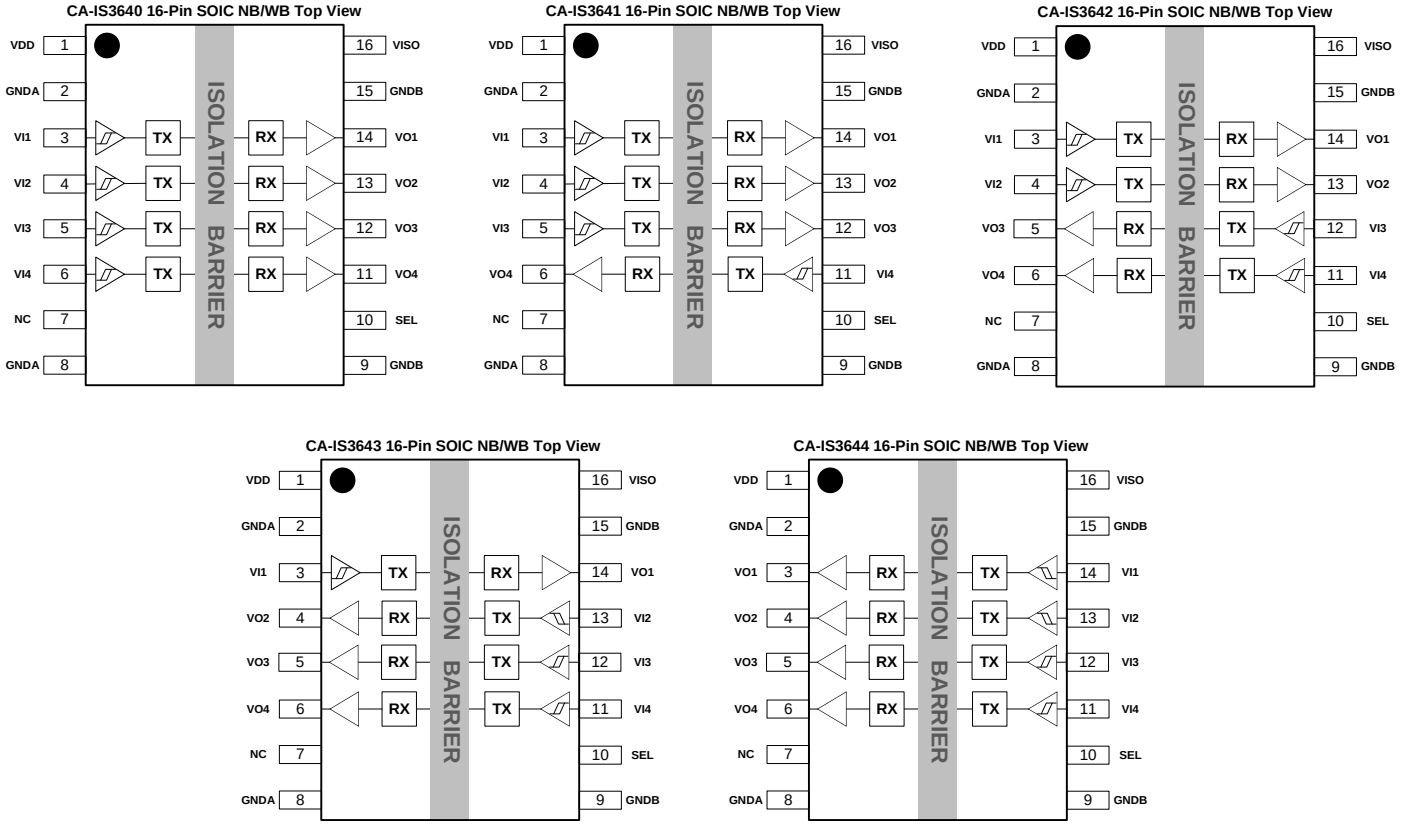


Figure 7-2 CA-IS364x Top View

Table 7-2 CA-IS364x Pin Description and Functions

Name	SOIC16 Pin#	Type	Description
VDD	1	Supply Input	Side A power supply
GNDA	2	Ground	Side A ground
VI1 / VO1	3	Digital I/O	Side A digital input for CA-IS3640 / CA-IS3641 / CA-IS3642 / CA-IS3643 or output for CA-IS3644
VI2 / VO2	4	Digital I/O	Side A digital input for CA-IS3640 / CA-IS3641 / CA-IS3642 or output for CA-IS3643 / CA-IS3644
VI3 / VO3	5	Digital I/O	Side A digital input for CA-IS3640 / CA-IS3641 or output for CA-IS3642 / CA-IS3643 / CA-IS3644
VI4 / VO4	6	Digital I/O	Side A digital input for CA-IS3640 or output for CA-IS3641 / CA-IS3642 / CA-IS3643 / CA-IS3644
NC[1]	7	No Connection	Not Connected
GNDA	8	Ground	Side A ground
GNDB	9	Ground	Side B ground
SEL[2]	10	Digital Input	VISO selection pin
VI4 / VO4	11	Digital I/O	Side B digital input for CA-IS3641 / CA-IS3642 / CA-IS3643 / CA-IS3644 or output for CA-IS3640
VI3 / VO3	12	Digital I/O	Side B digital input for CA-IS3642 / CA-IS3643 / CA-IS3644 or output for CA-IS3640 / CA-IS3641
VI2 / VO2	13	Digital I/O	Side B digital input for CA-IS3643 / CA-IS3644 or output for CA-IS3640 / CA-IS3641 / CA-IS3642
VI1 / VO1	14	Digital I/O	Side B digital input for CA-IS3644 or output for CA-IS3640 / CA-IS3641 / CA-IS3642 / CA-IS3643
GNDB	15	Ground	Side B ground
VISO	16	Supply Output	Isolated output supply voltage determined by SEL pin

1. No Connect. These pins are not internally connected. They can be left floating, tied to VDD or tied to GND.
2. VISO selection pin. VISO = 5 V when SEL is connected to VISO. VISO = 3.3 V, when SEL is connected to GNDA or left floating. SEL operation is summarized in Table 10-1.

8 Specifications

8.1 Absolute Maximum Ratings[1, 2]

		MIN	MAX	UNIT
V_{DD}	Supply voltage	-0.5	6.0	V
V_{ISO}	Isolated supply Voltage	-0.5	6.0	V
V_{in}	Voltage at Ax, Bx, ENx	-0.5	V_{DDA}+0.5[3]	V
I_O	Output current	-20	20	mA
T_J	Junction temperature		150	°C
T_{STG}	Storage temperature	-65	150	°C

NOTE:

1. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GNDA or GNDB) and are peak voltage values.
3. Maximum voltage must not exceed 6 V.

8.2 ESD Ratings

		VALUE	UNIT
V_{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±1000	

NOTE:

1. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
2. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

			MIN	TYP	MAX	UNIT
V_{DD}	Supply Voltage		3		5.5	V
I_{OH}	High-level Output Current	V_{DDO}[1] = 5V	-4			mA
		V_{DDO} = 3.3V	-2			
		V_{DDO} = 2.5V	-1			
I_{OL}	Low-level Output Current	V_{DDO} = 5V			4	mA
		V_{DDO} = 3.3V			2	
		V_{DDO} = 2.5V			1	
V_{IH}	High-level Input Voltage		2.0			V
V_{IL}	Low-level Input Voltage				0.8	V
DR	Data Rate		0		150	Mbps
T_A	Ambient Temperature		-55	27	125	°C

NOTE:

1. V_{DDO} = Output-side V_{DD}

8.4 Thermal Information

THERMAL METRIC		CA-IS36xx W (SOIC) 16 Pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.4	°C/W

8.5 Power Rating

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum Power Dissipation				1	W
P_{DA}	Maximum Power Dissipation on Side-A				0.5	W
P_{DB}	Maximum Power Dissipation on Side-B				0.5	W

8.6 Insulation Specifications

PARAMETR		TEST CONDITIONS	VALUE W	UNIT
CLR	External clearance[1]	Shortest terminal-to-terminal distance through air	8	mm
CPG	External creepage[1]	Shortest terminal-to-terminal distance across the package surface	8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	19	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 400 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-III	
DIN V VDE V 0884-11:2017-01[2]				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	849	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDB) Test	600	V_{RMS}
		DC voltage	849	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t= 1 s (100% production)	7070	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[3]	Test method per IEC 60065, 1.2/50 µs waveform, $V_{TEST} = 1.6 \times V_{IOSM}$ (qualification)	6250	V_{PK}
q_{pd}	Apparent charge[4]	Method a, After Input/Output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤5	pC
		Method a, After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤5	
		Method b1, At routine test (100% production) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	≤5	
C_{IO}	Barrier capacitance, input to output[5]	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	~0.5	pF
R_{IO}	Isolation resistance[5]	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	
	Pollution degree		2	
UL 1577				
V_{ISO}	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	5000	V_{RMS}

NOTE:

1. Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
2. This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
3. Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
4. Apparent charge is electrical discharge caused by a partial discharge (pd).
5. All pins on each side of the barrier tied together creating a two-terminal device.

8.7 Safety-Related Certifications

VDE(Pending)	CSA(Pending)	UL(Pending)	CQC(Pending)	TUV(Pending)
Certified according to DIN V VDE V 0884-11:2017-01	Certified according to IEC 60950-1, IEC 62368-1 and IEC 60601-1	Recognized under UL 1577 Component Recognition Program	Certified according to GB4943.1-2011	Certified according to EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A2:2013

8.8 Electrical Characteristics

8.8.1 5 V Input, 5 V output

V_{DD}= 5 V ± 10%, T_A = -55 to 125°C, SEL shorted to V_{ISO}

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ISO}	Isolated supply voltage	External I_{ISO} = 0 to 50 mA	4.75	5.07	5.43	V
		External I_{ISO} = 0 to 130 mA	4.5	5.07	5.43	
$V_{ISO(LINE)}$	DC line regulation	I_{ISO} = 50 mA, V_{DD} = 4.5 V to 5.5 V		2		mV/V
$V_{ISO(LOAD)}$	DC load regulation	I_{ISO} = 0 to 130 mA		1%		
EFF	Efficiency at maximum load current	I_{ISO} = 130 mA, C_{LOAD} = 0.1 µF || 10 µF; V_I = V_{DDI}[1] (CA-IS36xxL); V_I = 0 V (CA-IS36xxH)		53%		
$V_{DD(UVLO+)}$	VDD undervoltage threshold when supply voltage is rising				2.7	V
$V_{DD(UVLO-)}$	VDD undervoltage threshold when supply voltage is falling		2.1			V
$V_{HYS(UVLO)}$	VDD undervoltage threshold hysteresis			0.2		V
$V_{IT+(IN)}$	Positive-going input threshold		1.4	1.67	1.9	V
$V_{IT-(IN)}$	Negative-going input threshold		1.0	1.23	1.4	V
$V_{I(HYS)}$	Input threshold hysteresis		0.30	0.44	0.50	V
I_{IH}	High-level input leakage current	V_{IH} = V_{DDI}[1] at Ax or Bx or ENx or SEL			15	µA
I_{IL}	Low-level input leakage current	V_{IL} = 0 V at Ax or Bx or ENx or SEL	-15			µA
V_{OH}	High-level output voltage	I_{OH} = -4mA; *See Figure 9-1*	V_{DDO}[1]-0.4	V_{DDO}-0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 4mA; *See Figure 9-1*		0.2	0.4	V
CMTI	Common-mode transient immunity	V_I = V_{DDI}[1] or 0 V, V_{CM} = 1500 V; *See Figure 9-2*	100	150		kV/µS
I_{SCC_SC}	DC current from supply under short circuit on V_{ISO}	V_{ISO} shorted to GNDB		137		mA
$V_{ISO(RIP)}$	Output ripple on isolated supply (pk-pk)			100		mV

Note:
1. V_{DDI} = input side supply; V_{DDO} = output side supply

8.8.2 5 V Input, 3.3V Output

V_{DD}= 5 V ± 10%, T_A = -55 to 125°C, SEL shorted to GNDB

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ISO}	Isolated supply voltage	External I_{ISO} = 0 to 50 mA	3.13	3.34	3.56	V
		External I_{ISO} = 0 to 130 mA	3	3.34	3.56	
$V_{ISO(LINE)}$	DC line regulation	I_{ISO} = 50 mA, V_{DD} = 4.5 V to 5.5 V		2		mV/V
$V_{ISO(LOAD)}$	DC load regulation	I_{ISO} = 0 to 130 mA		1%		
EFF	Efficiency at maximum load current	I_{ISO} = 130 mA, C_{LOAD} = 0.1 µF || 10 µF; V_I = V_{DDI}[1] (CA-IS36xxL); V_I = 0 V (CA-IS36xxH)		48%		
$V_{DD(UVLO+)}$	VDD undervoltage threshold when supply voltage is rising				2.7	V
$V_{DD(UVLO-)}$	VDD undervoltage threshold when supply voltage is falling		2.1			V
$V_{HYS(UVLO)}$	VDD undervoltage threshold hysteresis			0.2		V
$V_{IT+(IN)}$	Positive-going input threshold		1.4	1.67	1.9	V
$V_{IT-(IN)}$	Negative-going input threshold		1.0	1.23	1.4	V
$V_{I(HYS)}$	Input threshold hysteresis		0.30	0.44	0.50	V
I_{IH}	High-level input leakage current	V_{IH} = V_{DDI}[1] at Ax or Bx or ENx or SEL			15	µA
I_{IL}	Low-level input leakage current	V_{IL} = 0 V at Ax or Bx or ENx or SEL	-15			µA
V_{OH}	High-level output voltage	I_{OH} = -4mA; *See Figure 9-1*	V_{DDO}[1]-0.4	V_{DDO}-0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 4mA; *See Figure 9-1*		0.2	0.4	V
CMTI	Common-mode transient immunity	V_I = V_{DDI}[1] or 0 V, V_{CM} = 1500 V; *See Figure 9-2*	100	150		kV/µS
I_{SCC_SC}	DC current from supply under short circuit on V_{ISO}	V_{ISO} shorted to GNDB		137		mA
$V_{ISO(RIP)}$	Output ripple on isolated supply (pk-pk)			100		mV

Note:
1. V_{DDI} = input side supply; V_{DDO} = output side supply

8.8.3 3.3V Input, 3.3 V Output

V_{DD}= 3.3 V ± 10%, T_A = -55 to 125°C, SEL shorted to GNDB

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ISO}	Isolated supply voltage	External I_{ISO} = 0 to 50 mA	3.13	3.34	3.56	V
		External I_{ISO} = 0 to 130 mA	3	3.34	3.56	
$V_{ISO(LINE)}$	DC line regulation	I_{ISO} = 50 mA, V_{DD} = 4.5 V to 5.5 V		2		mV/V
$V_{ISO(LOAD)}$	DC load regulation	I_{ISO} = 0 to 130 mA		1%		
EFF	Efficiency at maximum load current	I_{ISO} = 130 mA, C_{LOAD} = 0.1 µF || 10 µF; V_I = V_{DDI}[1] (CA-IS36xxL); V_I = 0 V (CA-IS36xxH)		47%		
$V_{DD(UVLO+)}$	VDD undervoltage threshold when supply voltage is rising				2.7	V
$V_{DD(UVLO-)}$	VDD undervoltage threshold when supply voltage is falling		2.1			V
$V_{HYS(UVLO)}$	VDD undervoltage threshold hysteresis			0.2		V
$V_{IT+(IN)}$	Positive-going input threshold		1.4	1.67	1.9	V
$V_{IT-(IN)}$	Negative-going input threshold		1.0	1.23	1.4	V
$V_{I(HYS)}$	Input threshold hysteresis		0.30	0.44	0.50	V
I_{IH}	High-level input leakage current	V_{IH} = V_{DDI}[1] at Ax or Bx or ENx or SEL			15	µA
I_{IL}	Low-level input leakage current	V_{IL} = 0 V at Ax or Bx or ENx or SEL	-15			µA
V_{OH}	High-level output voltage	I_{OH} = -4mA; *See Figure 9-1*	V_{DDO}[1]-0.4	V_{DDO}-0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 4mA; *See Figure 9-1*		0.2	0.4	V
CMTI	Common-mode transient immunity	V_I = V_{DDI}[1] or 0 V, V_{CM} = 1500 V; *See Figure 9-2*	100	150		kV/µS
I_{SCC_SC}	DC current from supply under short circuit on V_{ISO}	V_{ISO} shorted to GNDB		143		mA
$V_{ISO(RIP)}$	Output ripple on isolated supply (pk-pk)			90		mV

Note: 1. V_{DDI} = input side supply; V_{DDO} = output side supply.

8.9 Supply Current Characteristics

8.9.1 5 V Input, 5 V Output

V_{DD}= 5 V ± 10%, T_A = -55 to 125°C, SEL shorted to V_{ISO}

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
CA-IS3620						
I_{DD}	Current drawn from supply	No external I_{LOAD}; V_I = 0 V (CA-IS3620H); V_I = V_{DDI}[1] (CA-IS3620L)		21		mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3620L); V_I = V_{DDI}[1] (CA-IS3620H)		17		
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		19		
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		20		
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		33		
$I_{ISO(OUT)}$	Current available to isolated supply	No external I_{LOAD}; V_I = 0 V (CA-IS3620H); V_I = V_{DDI}[1] (CA-IS3620L)	127			mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3620L); V_I = V_{DDI}[1] (CA-IS3620H)	130			
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	128			
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	128			
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	125			
CA-IS3621						
I_{DD}	Current drawn from supply	No external I_{LOAD}; V_I = 0 V (CA-IS3621H); V_I = V_{DDI}[1] (CA-IS3621L)		22		mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3621L); V_I = V_{DDI}[1] (CA-IS3621H)		16		
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		19		
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		20		
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		30		
$I_{ISO(OUT)}$	Current available to isolated supply	No external I_{LOAD}; V_I = 0 V (CA-IS3621H); V_I = V_{DDI}[1] (CA-IS3621L)	127			mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3621L); V_I = V_{DDI}[1] (CA-IS3621H)	130			
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	128			
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	128			
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	126			

Note:

1. V_{DDI} = Input-side V_{DD}

Supply Current Characteristics Continued (5 V Input, 5 V Output)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
CA-IS3622						
I_{DD}	Current drawn from supply	No external I_{LOAD}; V_I = 0 V (CA-IS3622H); V_I = V_{DDI}[1] (CA-IS3622L)		22		mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3622L); V_I = V_{DDI}[1] (CA-IS3622H)		16		
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		19		
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		20		
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		30		
$I_{ISO(OUT)}$	Current available to isolated supply	No external I_{LOAD}; V_I = 0 V (CA-IS3622H); V_I = V_{DDI}[1] (CA-IS3622L)	127			mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3622L); V_I = V_{DDI}[1] (CA-IS3622H)	130			
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	128			
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	128			
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	126			
CA-IS3640						
I_{DD}	Current drawn from supply	No external I_{LOAD}; V_I = 0 V (CA-IS3640H); V_I = V_{DDI}[1] (CA-IS3640L)		23		mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3640L); V_I = V_{DDI}[1] (CA-IS3640H)		17		
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		21		
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		24		
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		56		
$I_{ISO(OUT)}$	Current available to isolated supply	No external I_{LOAD}; V_I = 0 V (CA-IS3640H); V_I = V_{DDI}[1] (CA-IS3640L)	128			mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3640L); V_I = V_{DDI}[1] (CA-IS3640H)	130			
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	128			
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	127			
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	111			
CA-IS3641						
I_{DD}	Current drawn from supply	No external I_{LOAD}; V_I = 0 V (CA-IS3641H); V_I = V_{DDI}[1] (CA-IS3641L)		23		mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3641L); V_I = V_{DDI}[1] (CA-IS3641H)		17		
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		20		
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		24		
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		54		
$I_{ISO(OUT)}$	Current available to isolated supply	No external I_{LOAD}; V_I = 0 V (CA-IS3641H); V_I = V_{DDI}[1] (CA-IS3641L)	128			mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3641L); V_I = V_{DDI}[1] (CA-IS3641H)	130			
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	128			
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	127			
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	112			

Note: 1. V_{DDI} = Input-side V_{DD}

Supply Current Characteristics Continued (5 V Input, 5 V Output)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
CA-IS3642						
I_{DD}	Current drawn from supply	No external I_{LOAD}; V_I = 0 V (CA-IS3642H); V_I = V_{DDI}[1] (CA-IS3642L)		24		mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3642L); V_I = V_{DDI}[1] (CA-IS3642H)		18		
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		21		
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		24		
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		51		
$I_{ISO(OUT)}$	Current available to isolated supply	No external I_{LOAD}; V_I = 0 V (CA-IS3642H); V_I = V_{DDI}[1] (CA-IS3642L)	126			mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3642L); V_I = V_{DDI}[1] (CA-IS3642H)	130			
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	128			
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	127			
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	116			
CA-IS3643						
I_{DD}	Current drawn from supply	No external I_{LOAD}; V_I = 0 V (CA-IS3643H); V_I = V_{DDI}[1] (CA-IS3643L)		25		mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3643L); V_I = V_{DDI}[1] (CA-IS3643H)		17		
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		21		
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		24		
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		48		
$I_{ISO(OUT)}$	Current available to isolated supply	No external I_{LOAD}; V_I = 0 V (CA-IS3643H); V_I = V_{DDI}[1] (CA-IS3643L)	125			mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3643L); V_I = V_{DDI}[1] (CA-IS3643H)	130			
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	127			
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	126			
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	120			
CA-IS3644						
I_{DD}	Current drawn from supply	No external I_{LOAD}; V_I = 0 V (CA-IS3644H); V_I = V_{DDI}[1] (CA-IS3644L)		26		mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3644L); V_I = V_{DDI}[1] (CA-IS3644H)		17		
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		22		
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		24		
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		46		
$I_{ISO(OUT)}$	Current available to isolated supply	No external I_{LOAD}; V_I = 0 V (CA-IS3644H); V_I = V_{DDI}[1] (CA-IS3644L)	127			mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3644L); V_I = V_{DDI}[1] (CA-IS3644H)	130			
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	128			
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	128			
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	125			

Note: 1. V_{DDI} = Input-side V_{DD}

8.9.2 5 V Input, 3.3 V Output

V_{DD}= 5 V ± 10%, T_A = -55 to 125°C, SEL shorted to GNDB

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
CA-IS3620						
I_{DD}	Current drawn from supply	No external I_{LOAD}; V_I = 0 V (CA-IS3620H); V_I = V_{DDI}[1] (CA-IS3620L)		17		mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3620L); V_I = V_{DDI}[1] (CA-IS3620H)		14		
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		16		
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		17		
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		27		
$I_{ISO(OUT)}$	Current available to isolated supply	No external I_{LOAD}; V_I = 0 V (CA-IS3620H); V_I = V_{DDI}[1] (CA-IS3620L)	127			mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3620L); V_I = V_{DDI}[1] (CA-IS3620H)	130			
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	128			
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	128			
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	126			
CA-IS3621						
I_{DD}	Current drawn from supply	No external I_{LOAD}; V_I = 0 V (CA-IS3621H); V_I = V_{DDI}[1] (CA-IS3621L)		18		mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3621L); V_I = V_{DDI}[1] (CA-IS3621H)		13		
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		16		
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		17		
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		24		
$I_{ISO(OUT)}$	Current available to isolated supply	No external I_{LOAD}; V_I = 0 V (CA-IS3621H); V_I = V_{DDI}[1] (CA-IS3621L)	127			mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3621L); V_I = V_{DDI}[1] (CA-IS3621H)	130			
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	128			
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	128			
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	126			

Note:
1. V_{DDI} = Input-side V_{DD}

Supply Current Characteristics Continued (5 V Input, 3.3 V Output)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
CA-IS3622						
I_{DD}	Current drawn from supply	No external I_{LOAD}; V_I = 0 V (CA-IS3622H); V_I = V_{DDI}[1] (CA-IS3622L)		18		mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3622L); V_I = V_{DDI}[1] (CA-IS3622H)		13		
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		16		
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		17		
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		24		
$I_{ISO(OUT)}$	Current available to isolated supply	No external I_{LOAD}; V_I = 0 V (CA-IS3622H); V_I = V_{DDI}[1] (CA-IS3622L)	127			mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3622L); V_I = V_{DDI}[1] (CA-IS3622H)	130			
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	128			
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	128			
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	126			
CA-IS3640						
I_{DD}	Current drawn from supply	No external I_{LOAD}; V_I = 0 V (CA-IS3640H); V_I = V_{DDI}[1] (CA-IS3640L)		20		mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3640L); V_I = V_{DDI}[1] (CA-IS3640H)		15		
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		17		
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		19		
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		39		
$I_{ISO(OUT)}$	Current available to isolated supply	No external I_{LOAD}; V_I = 0 V (CA-IS3640H); V_I = V_{DDI}[1] (CA-IS3640L)	128			mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3640L); V_I = V_{DDI}[1] (CA-IS3640H)	130			
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	129			
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	128			
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	116			
CA-IS3641						
I_{DD}	Current drawn from supply	No external I_{LOAD}; V_I = 0 V (CA-IS3641H); V_I = V_{DDI}[1] (CA-IS3641L)		23		mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3641L); V_I = V_{DDI}[1] (CA-IS3641H)		14		
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		17		
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		20		
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		40		
$I_{ISO(OUT)}$	Current available to isolated supply	No external I_{LOAD}; V_I = 0 V (CA-IS3641H); V_I = V_{DDI}[1] (CA-IS3641L)	128			mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3641L); V_I = V_{DDI}[1] (CA-IS3641H)	130			
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	129			
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	128			
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	118			

Note: 1. V_{DDI} = Input-side V_{DD}

Supply Current Characteristics Continued (5 V Input, 3.3 V Output)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
CA-IS3642						
I_{DD}	Current drawn from supply	No external I_{LOAD}; V_I = 0 V (CA-IS3642H); V_I = V_{DDI}[1] (CA-IS3642L)		20		mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3642L); V_I = V_{DDI}[1] (CA-IS3642H)		15		
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		18		
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		20		
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		39		
$I_{ISO(OUT)}$	Current available to isolated supply	No external I_{LOAD}; V_I = 0 V (CA-IS3642H); V_I = V_{DDI}[1] (CA-IS3642L)	126			mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3642L); V_I = V_{DDI}[1] (CA-IS3642H)	130			
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	128			
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	127			
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	119			
CA-IS3643						
I_{DD}	Current drawn from supply	No external I_{LOAD}; V_I = 0 V (CA-IS3643H); V_I = V_{DDI}[1] (CA-IS3643L)		20		mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3643L); V_I = V_{DDI}[1] (CA-IS3643H)		14		
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		18		
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		20		
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		39		
$I_{ISO(OUT)}$	Current available to isolated supply	No external I_{LOAD}; V_I = 0 V (CA-IS3643H); V_I = V_{DDI}[1] (CA-IS3643L)	125			mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3643L); V_I = V_{DDI}[1] (CA-IS3643H)	130			
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	127			
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	127			
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	123			
CA-IS3644						
I_{DD}	Current drawn from supply	No external I_{LOAD}; V_I = 0 V (CA-IS3644H); V_I = V_{DDI}[1] (CA-IS3644L)		21		mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3644L); V_I = V_{DDI}[1] (CA-IS3644H)		15		
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		18		
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		20		
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		41		
$I_{ISO(OUT)}$	Current available to isolated supply	No external I_{LOAD}; V_I = 0 V (CA-IS3644H); V_I = V_{DDI}[1] (CA-IS3644L)	123			mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3644L); V_I = V_{DDI}[1] (CA-IS3644H)	130			
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	126			
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	126			
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	126			

Note: 1. V_{DDI} = Input-side V_{DD}

8.9.3 3.3 V Input, 3.3 V Output

V_{DD}= 3.3 V ± 10%, T_A = -55 to 125°C, SEL shorted to GNDB

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
CA-IS3620						
I_{DD}	Current drawn from supply	No external I_{LOAD}; V_I = 0 V (CA-IS3620H); V_I = V_{DDI}[1] (CA-IS3620L)		24		mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3620L); V_I = V_{DDI}[1] (CA-IS3620H)		19		
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		22		
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		22		
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		22		
$I_{ISO(OUT)}$	Current available to isolated supply	No external I_{LOAD}; V_I = 0 V (CA-IS3620H); V_I = V_{DDI}[1] (CA-IS3620L)	72			mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3620L); V_I = V_{DDI}[1] (CA-IS3620H)	75			
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	75			
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	73			
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	71			
CA-IS3621						
I_{DD}	Current drawn from supply	No external I_{LOAD}; V_I = 0 V (CA-IS3621H); V_I = V_{DDI}[1] (CA-IS3621L)		25		mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3621L); V_I = V_{DDI}[1] (CA-IS3621H)		18		
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		22		
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		22		
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		19		
$I_{ISO(OUT)}$	Current available to isolated supply	No external I_{LOAD}; V_I = 0 V (CA-IS3621H); V_I = V_{DDI}[1] (CA-IS3621L)	72			mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3621L); V_I = V_{DDI}[1] (CA-IS3621H)	75			
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	75			
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	73			
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	71			

Note:

1. V_{DDI} = Input-side V_{DD}

Supply Current Characteristics Continued (3.3 V Input, 3.3 V Output)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
CA-IS3622						
I_{DD}	Current drawn from supply	No external I_{LOAD}; V_I = 0 V (CA-IS3622H); V_I = V_{DDI}[1] (CA-IS3622L)		25		mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3622L); V_I = V_{DDI}[1] (CA-IS3622H)		18		
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		22		
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		22		
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		19		
$I_{ISO(OUT)}$	Current available to isolated supply	No external I_{LOAD}; V_I = 0 V (CA-IS3622H); V_I = V_{DDI}[1] (CA-IS3622L)	72			mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3622L); V_I = V_{DDI}[1] (CA-IS3622H)	75			
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	75			
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	73			
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	71			
CA-IS3640						
I_{DD}	Current drawn from supply	No external I_{LOAD}; V_I = 0 V (CA-IS3640H); V_I = V_{DDI}[1] (CA-IS3640L)		26		mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3640L); V_I = V_{DDI}[1] (CA-IS3640H)		20		
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		23		
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		26		
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		54		
$I_{ISO(OUT)}$	Current available to isolated supply	No external I_{LOAD}; V_I = 0 V (CA-IS3640H); V_I = V_{DDI}[1] (CA-IS3640L)	73			mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3640L); V_I = V_{DDI}[1] (CA-IS3640H)	75			
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	74			
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	73			
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	61			
CA-IS3641						
I_{DD}	Current drawn from supply	No external I_{LOAD}; V_I = 0 V (CA-IS3641H); V_I = V_{DDI}[1] (CA-IS3641L)		23		mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3641L); V_I = V_{DDI}[1] (CA-IS3641H)		14		
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		17		
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		20		
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		40		
$I_{ISO(OUT)}$	Current available to isolated supply	No external I_{LOAD}; V_I = 0 V (CA-IS3641H); V_I = V_{DDI}[1] (CA-IS3641L)	73			mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3641L); V_I = V_{DDI}[1] (CA-IS3641H)	75			
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	74			
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	73			
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	61			

Note: 1. V_{DDI} = Input-side V_{DD}

Supply Current Characteristics Continued (3.3 V Input, 3.3 V Output)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
CA-IS3642						
I_{DD}	Current drawn from supply	No external I_{LOAD}; V_I = 0 V (CA-IS3642H); V_I = V_{DDI}[1] (CA-IS3642L)		20		mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3642L); V_I = V_{DDI}[1] (CA-IS3642H)		15		
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		18		
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		20		
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		39		
$I_{ISO(OUT)}$	Current available to isolated supply	No external I_{LOAD}; V_I = 0 V (CA-IS3642H); V_I = V_{DDI}[1] (CA-IS3642L)	73			mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3642L); V_I = V_{DDI}[1] (CA-IS3642H)	75			
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	73			
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	72			
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	64			
CA-IS3643						
I_{DD}	Current drawn from supply	No external I_{LOAD}; V_I = 0 V (CA-IS3643H); V_I = V_{DDI}[1] (CA-IS3643L)		20		mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3643L); V_I = V_{DDI}[1] (CA-IS3643H)		14		
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		18		
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		20		
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		39		
$I_{ISO(OUT)}$	Current available to isolated supply	No external I_{LOAD}; V_I = 0 V (CA-IS3643H); V_I = V_{DDI}[1] (CA-IS3643L)	70			mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3643L); V_I = V_{DDI}[1] (CA-IS3643H)	75			
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	72			
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	72			
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	68			
CA-IS3644						
I_{DD}	Current drawn from supply	No external I_{LOAD}; V_I = 0 V (CA-IS3644H); V_I = V_{DDI}[1] (CA-IS3644L)		21		mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3644L); V_I = V_{DDI}[1] (CA-IS3644H)		15		
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		18		
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		20		
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};		41		
$I_{ISO(OUT)}$	Current available to isolated supply	No external I_{LOAD}; V_I = 0 V (CA-IS3644H); V_I = V_{DDI}[1] (CA-IS3644L)	68			mA
		No external I_{LOAD}; V_I = 0 V (CA-IS3644L); V_I = V_{DDI}[1] (CA-IS3644H)	75			
		All channels switching with 50% duty cycle square wave clock input of 1Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	71			
		All channels switching with 50% duty cycle square wave clock input of 10Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	71			
		All channels switching with 50% duty cycle square wave clock input of 100Mbps; C_L = 15 pF for each channel, no external I_{LOAD};	71			

Note: 1. V_{DDI} = Input-side V_{DD}

8.10 Timing Characteristics

8.10.1 5 Input, 5V Output

V_{DD}= 5 V ± 10%, T_A = -55 to 125°C, SEL shorted to V_{ISO}

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DR	Data Rate		0		150	Mbps
PW_{min}	Minimum Pulse Width				5.0	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	*See Figure 9-1*	5.0	8.0	13.0	ns
PWD	Pulse Width Distortion $\|t_{PLH} - t_{PHL}\|$			0.2	4.5	ns
$t_{sk(o)}$	Channel-to-channel Output Skew Time[1]	Same-direction channels		0.4	2.5	ns
$t_{sk(pp)}$	Part-to-part Skew Time[2]			2.0	4.5	ns
t_r	Output Signal Rise Time	*See Figure 9-1*		2.5	4.0	ns
t_f	Output Signal Fall Time	*See Figure 9-1*		2.5	4.0	ns

NOTE:

1. $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected and the outputs switching in the same direction while driving identical loads.
2. $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

8.10.2 5 V Input, 3.3 V Output

V_{DD}= 5 V ± 10%, T_A = -55 to 125°C, SEL shorted to GNDB

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DR	Data Rate		0		150	Mbps
PW_{min}	Minimum Pulse Width				5.0	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	*See Figure 9-1*	5.0	8.0	13.0	ns
PWD	Pulse Width Distortion $\|t_{PLH} - t_{PHL}\|$			0.2	4.5	ns
$t_{sk(o)}$	Channel-to-channel Output Skew Time[1]	Same-direction channels		0.4	2.5	ns
$t_{sk(pp)}$	Part-to-part Skew Time[2]			2.0	4.5	ns
t_r	Output Signal Rise Time	*See Figure 9-1*		2.5	4.0	ns
t_f	Output Signal Fall Time	*See Figure 9-1*		2.5	4.0	ns

NOTE:

1. $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected and the outputs switching in the same direction while driving identical loads.
2. $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

8.10.3 3.3 V Input, 3.3 V Output

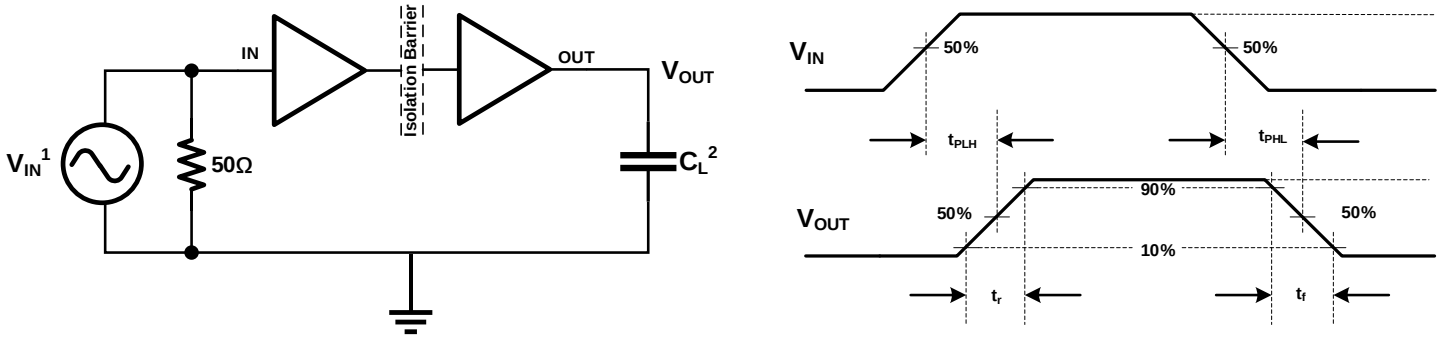
V_{DD}= 3.3 V ± 10%, T_A = -55 to 125°C, SEL shorted to GNDB

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DR	Data Rate		0		150	Mbps
PW_{min}	Minimum Pulse Width				5.0	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	*See Figure 9-1*	5.0	8.0	13.0	ns
PWD	Pulse Width Distortion $\|t_{PLH} - t_{PHL}\|$			0.2	4.5	ns
$t_{sk(o)}$	Channel-to-channel Output Skew Time[1]	Same-direction channels		0.4	2.5	ns
$t_{sk(pp)}$	Part-to-part Skew Time[2]			2.0	4.5	ns
t_r	Output Signal Rise Time	*See Figure 9-1*		2.5	4.0	ns
t_f	Output Signal Fall Time	*See Figure 9-1*		2.5	4.0	ns

NOTE:

1. $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected and the outputs switching in the same direction while driving identical loads.
2. $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

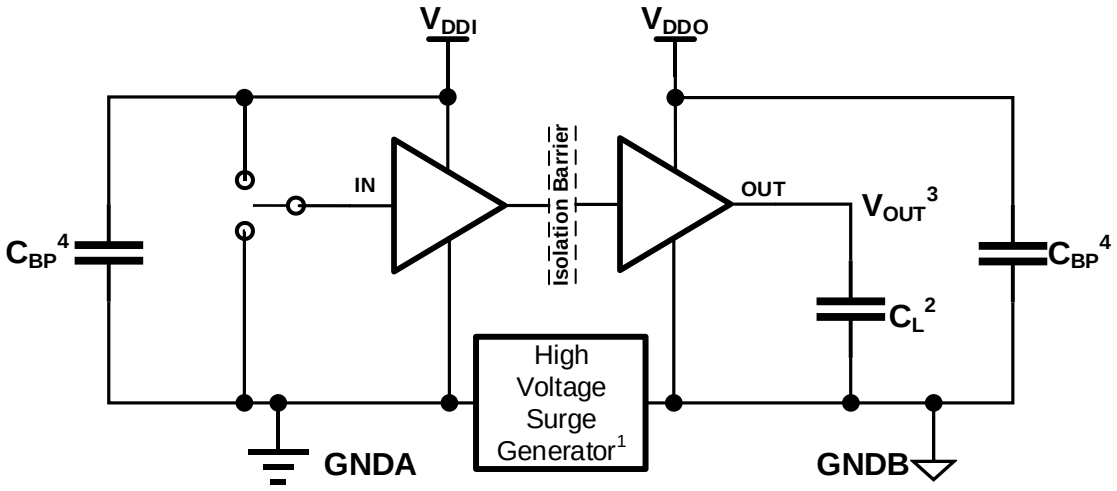
9 Parameter Measurement Information



NOTE:

1. A square wave generator generate the V_{IN} input signal with the following constraints: waveform frequency ⩽ 100kHz, 50% duty cycle, t_r⩽3ns, t_f⩽3ns. Since the waveform generator has an output impedance of Z_{out} = 50Ω, the 50Ω resistor in the figure is used for matching. There is no need in the actual application.
2. C_L is the load capacitance about 15pF together with the instrumentation capacitance. Since the load capacitance influence the output rising time, it's a key factor in the timing characteristic measurement.

Figure 9-1 Timing Characteristics Test Circuit and Voltage Waveforms



NOTE:

1. The High Voltage Surge Generator generates repetitive high voltage surges with > 1.5kV amplitude and <10ns rise time and fall time to reach common-mode transient noise with > 150kV/μs slew rate.
2. C_L is the load capacitance about 15pF together with the instrumentation capacitance.
3. Pass-fail criteria: The output must remain stable whenever the high voltage surges come.
4. C_{BP} is the 0.1 ~ 1uF bypass capacitance.

Figure 9-2 Common-Mode Transient Immunity Test Circuit

10 Detailed Description

10.1 Theory of Operation

The CA-IS36xx family of devices has a high-efficiency, low-emissions isolated dc-dc converter, with high-speed isolated data channels. The functional block diagram of CA-IS36xx devices are shown in Figure 10-1.

The dc-to-dc converter section of the CA-IS36xx devices works on principles that are common to most modern power supplies. The devices have a split controller architecture with isolated PWM feedback. V_{DD} power is supplied to an oscillating circuit that switches current into a high-Q on-chip air-core transformer which provide high efficiency and low radiated emissions. The integrated transformer uses thin film polymer as the insulation barrier. Power transferred to the secondary side is rectified and regulated to a value of 3.3 V or 5 V, depending on the setting of the SEL pin. The secondary (V_{ISO}) side controller regulates the output by creating a PWM control signal that is sent to the primary side by a dedicated isolated data channel. The PWM modulates the oscillator circuit to control the power being sent to the secondary side. Feedback allows for significantly higher power and efficiency and ensures low overshoots and undershoots during load transients. Undervoltage lockout (UVLO) with hysteresis is integrated on the V_{DD} and V_{ISO} supplies which ensures robust system performance under noisy conditions. An integrated soft-start mechanism ensures controlled inrush current and avoids any overshoot on the output during power up.

The high-speed isolated data channels use a simple ON-OFF keying (OOK) modulation scheme to transmit signal across the SiO_2 isolation capacitors that provide a robust insulation between two different voltage domain and act as a high frequency signal path between the input and the output. The transmitter (TX) modulates the input signal onto the carrier frequency, that is, TX delivers high frequency signal across the isolation barrier in one input state and delivers no signal across the barrier in the other input state. Then the receiver rebuilds the input signal according to the detected in-band energy. The capacitor-based signal path is fully differential to maximize noise immunity, which is also known as common-mode transient immunity. The capacitively-coupled architecture provides much higher electromagnetic immunity compared to the inductively coupled one. A simplified functional block diagram and conceptual operation waveforms of a single channel is shown in Figure 10-2 and Figure 10-3.

10.2 Functional Block Diagram

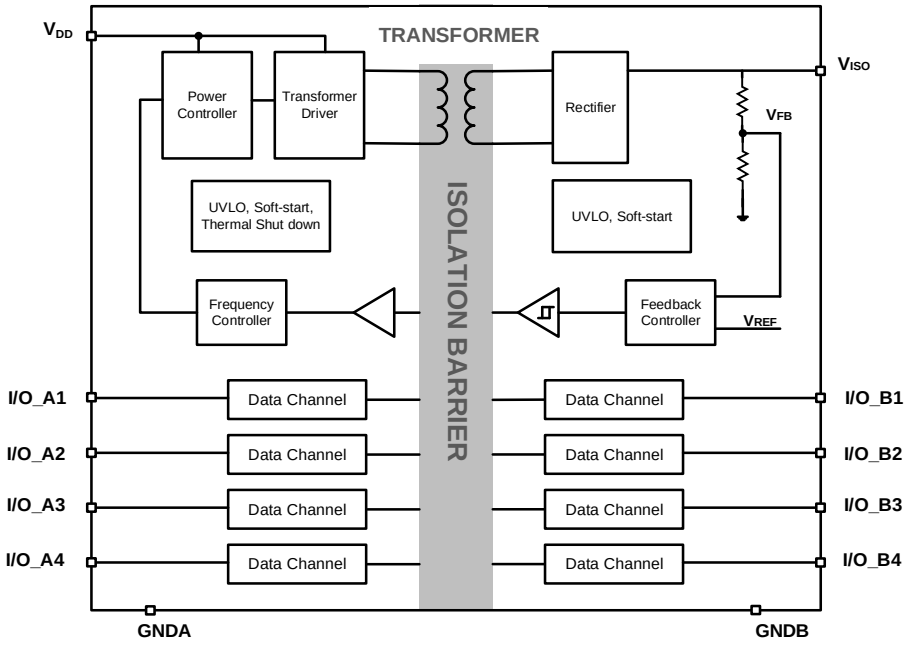


Figure 10-1 Functional Block Diagram of CA-IS36xx Devices

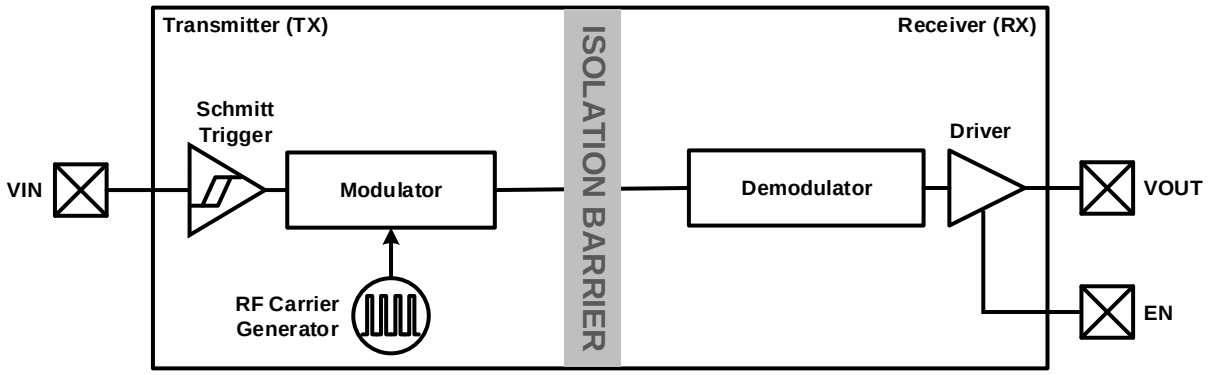


Figure 10-2 Functional Block Diagram of a Single Channel

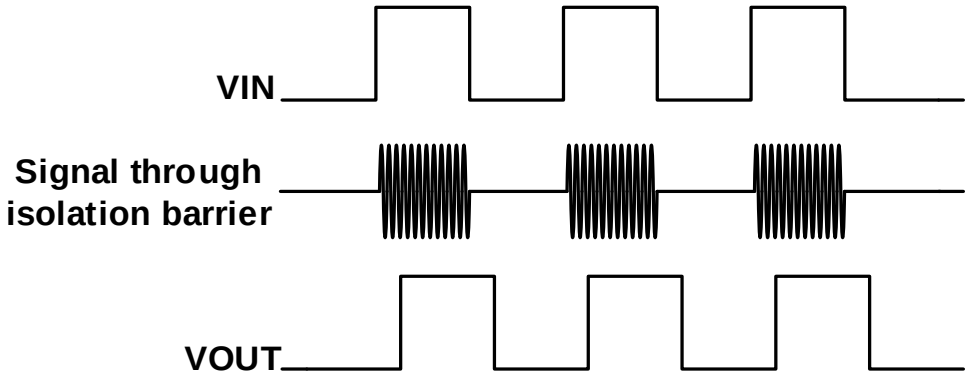


Figure 10-3 Conceptual Operation Waveforms of a Single Channel

10.3 Device Operation Modes

Table 10-1 provides the supply configurations for the CA-IS36x devices.

Table 10-1 Supply Configuration Table[1]

SEL INPUT	V_{DD}	V_{ISO}
Shorted to VISO	5 V	5V
Shorted to GNDB or floating	5 V	3.3V
Shorted to GNDB or floating	3.3 V[1]	3.3V[2]

Note:

1. V_{DD} = 3.3 V, SEL shorted to V_{ISO} (essentially V_{ISO} = 5 V) is not recommended mode of configuration.
2. The SEL pin has a weak pulldown internally. For V_{ISO} = 3.3 V, the SEL pin should be strongly connected to the GNDB pin in noisy system scenarios.

Table 10-2 provides the operation modes for the CA-IS36xx devices.

Table 10-2 Operation Mode Table[1]

V_{DD}	INPUT(Ax/Bx)[2]	OUTPUT (Ax/Bx)	OPERATION
PU	H	H	Normal operation mode: A channel's output follows the input state
	L	L	
	Open	Default	Default output fail-safe mode: If a channel's input is left open, its output goes to the default level. (Low for CA-IS36xxL and high for CA-IS36xxH)
PD	X	Undetermined[3]	

NOTE:
1. PU = Powered up (VDD ≥ 2.7 V); PD = Powered down (VDD ≤ 2.1 V); X = Irrelevant; H = High level; L = Low level.
2. The outputs are in undetermined state when V_{DD} < 2.1V.

Table 10-3 provides the Enable input truth table for the CA-IS362x devices.

Table 10-3 Enable Input Truth Table[1]

PART NUMBER	ENA[1]	OPERATION
CA-IS3621	H	Output A2 enabled and follows the input state.
	L	Output A2 disabled and in high impedance state[3].
CA-IS3622	H	Output A1 enabled and follows the input state.
	L	Output A1 disabled and in high impedance state[3].

NOTE:
1. H = high level; L = low level.
2. Enable inputs ENA can be used for multiplexing, for clock sync, or other output control. ENA logic operation is summarized for each isolator product in Table 10-3. This inputs is internally pulled-up to local V_{DD} allowing them to be connected to an external logic level (high or low) or left floating. To minimize noise coupling, do not connect circuit traces to ENA if it is left floating. If ENA is unused, it is recommended to be connected to an external logic level, especially if the CA-IS362x is operating in a noisy environment.
3. If a channel's output is in high impedance state, it goes to the default level. Low for CA-IS36xxL and high for CA-IS36xxH.

11 Application and Implementation

The devices require only external bypass capacitors to operate. These low-ESR ceramic bypass capacitors must be placed as close to the chip pads as possible. Figure 11-1 shows the typical application of CA-IS3642 device. And Figure 11-2 shows the typical schematic for SPI isolation using CA-IS3641 device.

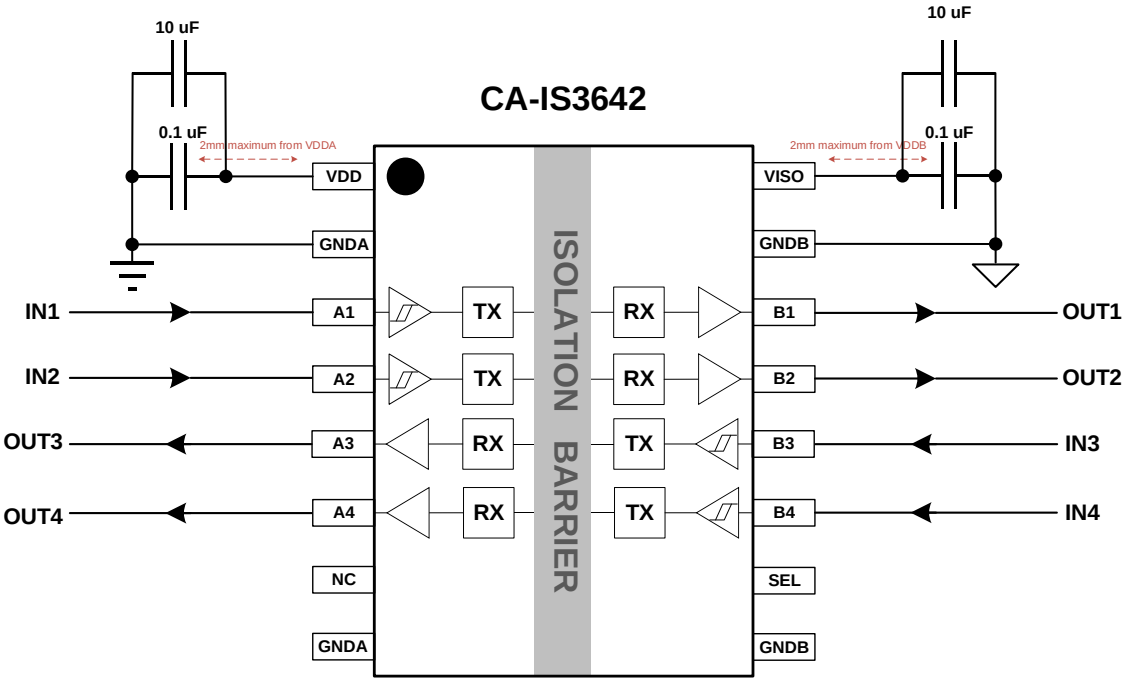


Figure 11-1 Typical Application Circuit of CA-IS3642

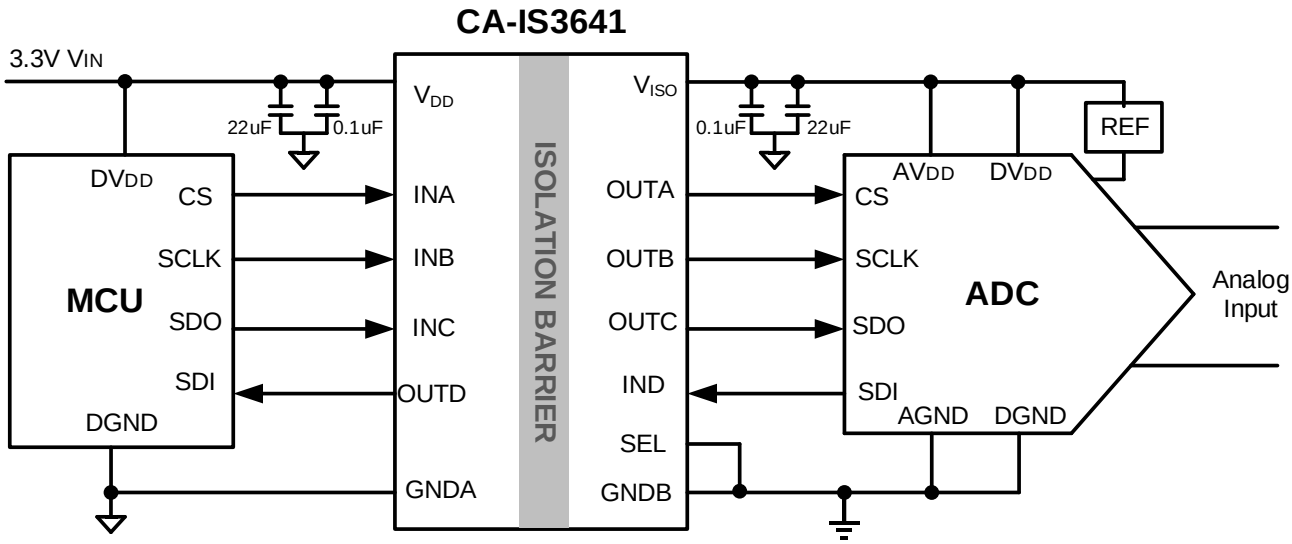
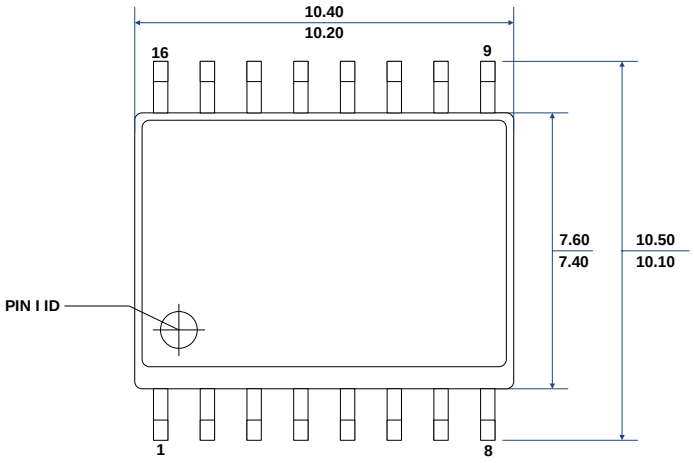


Figure 11-2 Isolated Power and SPI for ADC Sensing Application with ISOW7841

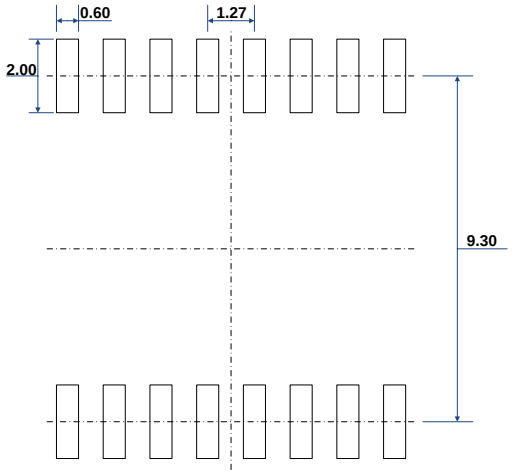
12 Package Information

12.1 16-Pin Wide Body SOIC Package

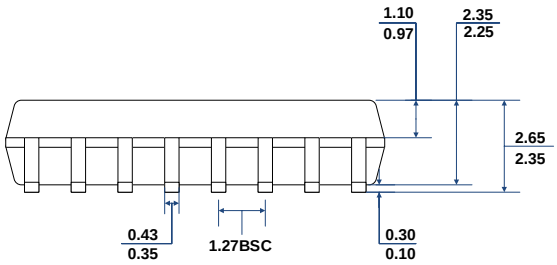
The figure below illustrates the package details and the recommended land pattern details for the CA-IS364x digital isolator in a 16-pin wide-body SOIC package. The values for the dimensions are shown in millimeters.



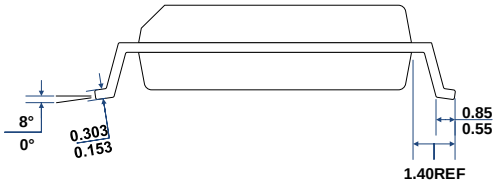
TOP VIEW



RECOMMENDED LAND PATTERN



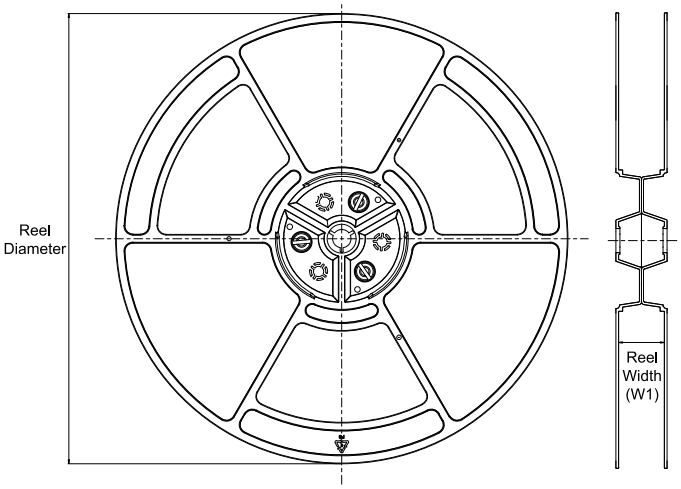
FRONT VIEW



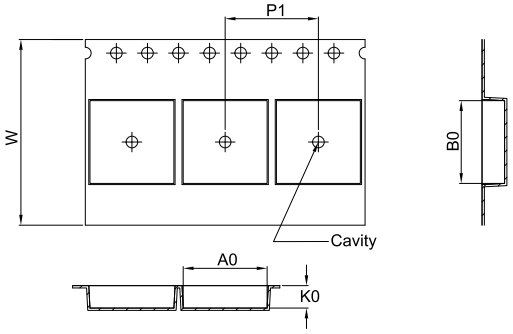
LEFT-SIDE VIEW

TAPE AND REEL INFORMATION

REEL DIMENSIONS

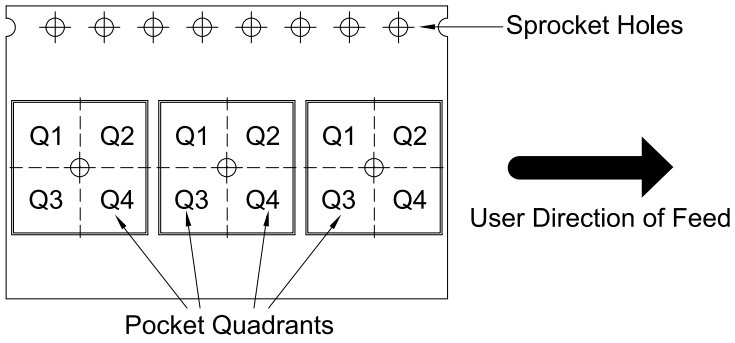


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS3620LW	SOIC	W	16	1000	330	16.4	10.8	10.7	2.9	12.0	24.0	Q1
CA-IS3620HW	SOIC	W	16	1000	330	16.4	10.8	10.7	2.9	12.0	24.0	Q1
CA-IS3621LW	SOIC	W	16	1000	330	16.4	10.8	10.7	2.9	12.0	24.0	Q1
CA-IS3621HW	SOIC	W	16	1000	330	16.4	10.8	10.7	2.9	12.0	24.0	Q1
CA-IS3622LW	SOIC	W	16	1000	330	16.4	10.8	10.7	2.9	12.0	24.0	Q1
CA-IS3622HW	SOIC	W	16	1000	330	16.4	10.8	10.7	2.9	12.0	24.0	Q1
CA-IS3640LW	SOIC	W	16	1000	330	16.4	10.8	10.7	2.9	12.0	24.0	Q1
CA-IS3640HW	SOIC	W	16	1000	330	16.4	10.8	10.7	2.9	12.0	24.0	Q1
CA-IS3641LW	SOIC	W	16	1000	330	16.4	10.8	10.7	2.9	12.0	24.0	Q1
CA-IS3641HW	SOIC	W	16	1000	330	16.4	10.8	10.7	2.9	12.0	24.0	Q1
CA-IS3642LW	SOIC	W	16	1000	330	16.4	10.8	10.7	2.9	12.0	24.0	Q1
CA-IS3642HW	SOIC	W	16	1000	330	16.4	10.8	10.7	2.9	12.0	24.0	Q1
CA-IS3643LW	SOIC	W	16	1000	330	16.4	10.8	10.7	2.9	12.0	24.0	Q1
CA-IS3643HW	SOIC	W	16	1000	330	16.4	10.8	10.7	2.9	12.0	24.0	Q1
CA-IS3644LW	SOIC	W	16	1000	330	16.4	10.8	10.7	2.9	12.0	24.0	Q1
CA-IS3644HW	SOIC	W	16	1000	330	16.4	10.8	10.7	2.9	12.0	24.0	Q1

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